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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/532,514	03/21/2000	MAKOTO KUDO	105803	6717

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EXAMINER	
FERRIS III, FRED O	

ART UNIT	PAPER NUMBER
2128	18

DATE MAILED: 02/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/532,514	Applicant(s) KUDO ET AL.	
	Examin r Fred Ferris	Art Unit 2123	

-- The MAILING DATE of this communication appears on the cover sheet with th corresp ndenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 December 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4, 6-23, and 25-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-4 and 6-18* is/are allowed.

6)☒ Claim(s) *19-23 and 25-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *10 October 2003* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10 October 2003 (paper # 14) has been entered. Claims 1-4, 6-23, and 25-28 are currently pending in this application. Applicants have cancelled claims 5 and 24. Claims 1-4 and 6-18 have now been allowed. Claims 19-23 and 25-28 remain rejected.

Response to Arguments

2. Applicant's arguments filed on 10 October 2003 (paper # 14) have been fully considered.

Regarding proposed drawing changes: The proposed drawing changes to Figures 1A and 1B have been approved by the examiner pending review by the draftsperson.

Regarding claimed subject matter: Applicant's have amended claims to include limitations drawn to the terminals between the product and emulation device. The examiner has withdrawn the 112(2) rejection and objection to the specification.

Regarding applicants response to 102(b) rejection: The examiner withdraws the 102(b) rejection of claim 1 in view of the amendment to the claims. However, the examiner maintains the 102(b) rejection of claims 19 and 20. While applicants have

argued that the prior art (Kai) does not disclose the bus control means (for) or a memory control means (for) of the claimed invention, the examiner notes that independent claims 19 and 20 do not recite "means for" language relating to the memory control or bus control process. Accordingly, these claims do not invoke 35 U.S.C. 112, paragraph 6. Therefore, since the claims do not specifically define otherwise, the examiner has interpreted the memory control process and the bus control process to be functionally equivalent to that disclosed in the prior art. This includes the multiple control signals (i.e. first, second, etc.) Applicants also argue that Kai does not disclose an external terminal connected to an emulation memory (emulation mode on) and an external memory (emulation mode off). The examiner asserts that the term "external terminal" is not specifically defined by the claim. Accordingly, the examiner interprets the external terminal to simply be an external bus connector that is functionally equivalent to the interconnect bus disclosed by Kai. (i.e. any external bus would inherently have an connector (external terminal) for connecting additional external memory and peripherals) Applicants further argue that Kai fails to disclose an external bus "connectable" to both an emulation memory and an external memory or a memory controller with control signals for connecting between internal memory, emulation, and external memory. The examiner asserts that Kai clearly discloses an interconnect bus (external) that is connectable to either an emulation memory (Fig. 1) or additional peripherals or memory (CL2-L37-54). Kai further discloses the necessary memory control signals (CL4-L10-37) and emulation mode on/of control (CL4-L4, 38-57). (please

see Kai Fig. 2 and 102(b) rejection) Accordingly, the examiner maintains the 102(b) rejection of claims 19 and 20.

Regarding applicants response to 103(a) rejection: The examiner withdraws the 103(a) rejection of claims 1-4 and 6-18 in view of applicant's amendment to the claims. However, the examiner maintains the 103(a) rejection of claims 19-23 and 25-28. Applicants have again argued that the prior art (Pawlowski or Gebhardt) does not disclose the bus control means (for) or a memory control means (for) of the claimed invention. The examiner again notes that independent claims 19 and 20 do not recite "means for" language relating to the memory control or bus control process. Accordingly, these claims do not invoke 35 U.S.C. 112, paragraph 6. Therefore, since the claims do not specifically define otherwise, the examiner has interpreted the memory control process and the bus control process to be functionally equivalent to that disclosed in the prior art. This includes the multiple control signals (i.e. first, second, etc.) as cited below under 103(a) rejections.

Applicants also argue that prior art (Pawlowski or Gebhardt) does not disclose an external terminal connected to an emulation memory (emulation mode on) and an external memory (emulation mode off). The examiner asserts that the term "external terminal" is not specifically defined by the claim. Accordingly, the examiner interprets the external terminal to simply be an external bus connector that is functionally equivalent to the bus systems disclosed by Pawlowski and Gebhardt.

Applicants have also argued the features relating to the operation of emulation mode (on/off) and optimization of the number of terminals in the microcomputer are

distinguishable over the prior art by referencing the specification page 10, line 27 to page 12, line 9. The examiner asserts that, although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See In re Van Geuns, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Accordingly, the examiner has interpreted these limitations as cited under the 103(a) rejections below.

The examiner disagrees with applicant's statement that prior art (Pawloski 618') teaches away from the features of the claimed invention because it incorporates two processors. This analysis appears piecemeal. One cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See In re Keller, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); In re Merck & Co., 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). The examiner asserts that Pawloski 618' discloses the cited features of the claimed invention as a subset and, hence, does not teach away from the limitations claimed invention. (please see 103(a) rejections below)

Applicants have also argued that examiners statement on page 4 of the Final Office Action relating to microprocessors including external memory and having different control signals is conclusory and provides no support. The examiner respectfully disagrees. The examiner clearly stated the these features are obvious and well-known in the art ***in addition to being clearly anticipated in the prior art,*** *and specifically cited where in the referenced prior art support for the these teachings can be found. Specifically, page 4, line 6 of the Final Office Action recites: "(i.e. external bus and memory will include multiple (different) control signals such as* ***those of Pawloski, Fig.***

Fig. 5D) (Also see G phardt – U.S. 4,939,637 Fig. 2, 3, 7)". The examiner further notes that, while the examiner has not taken Official Notice in this case, applicants claimed limitations (claims 19 & 20) relating to a microprocessors external bus and bus / memory control are sufficiently broad to be taught by nearly any of popular microcomputer bus standards including, VME bus, MULTI bus, IEEE 488 bus, etc.

The examiner maintains the 103(a) rejection of claims 19-23 and 25-28.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. The term "on production" in claim 19 is a relative term which renders the claim indefinite. The term "on production" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. Specifically, the term "on production" appears to refer to an emulation production "phase" but it is unclear which production phase (step) is being referenced (i.e. programming, manufacturing, or testing, etc.).

Claim 19 recites the limitation "said external terminals" in line 4. There is insufficient antecedent basis for this limitation in the claim. Line 2 on the claim 19 refers to "external signals" for an external bus. The examiner believes that applicants intended this term to be "external terminals" and not external signals as recited in the claim language. Corrective action is required.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 19, and 20 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by U.S. Patent 6,240,377 issued to Kai et al.

Regarding independent claims 19, and 20: Kai teaches a microcomputer based emulation system including a bus controller having an internal memory that also accesses an external bus, which includes an emulation memory, and executes an emulation mode. (Abstract, Summary of Invention, CL3-L37-60, CL4-L4, 10-57, Figs. 1-3) Kai further discloses an interconnect bus (external) that is connectable to either an emulation memory (Fig. 1) or additional peripherals or memory (CL2-L37-54). Kai also discloses the necessary memory control signals (CL4-L10-37) and emulation mode on/of control (CL4-L4, 38-57).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. ***Claims 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,313,618 issued to Pawlowski in view of U.S. Patent 5,623,673 issued to Gephardt et al.***

Independent claims 19 and 20 are drawn to:
A ***microcomputer and emulation method*** *for performing information processing and:*
A ***processor*** *for executing instructions*
External bus *connectable to* ***emulation memory*** *and* ***external memory***
Bus control *for connecting* ***processor to external bus*** *(from internal memory to emulation memory) in* ***emulation mode***

Regarding independent claims 19 and 20: Claims 19 and 20 are drawn to an emulation method and microcomputer and bus control that allows the processor to access an emulation memory and an external memory via an external bus that is switched from its internal memory via control signals. This technique is well known and in common use in the art. By way of example, Pawloski teaches a microcomputer (8051) having an ***internal memory*** *that also accesses an* ***external bus****, which includes an* ***emulation memory*** *and an external (RAM) memory. (Figs. 1, 2, CL1-L49) The microcomputer* ***controls*** *access the external bus by writing to* ***registers*** *(ports including dedicated* ***pins (terminals)****, CL10-L3) for selecting between memories and entering the*

***emulation mode**. (CL4-24) While Pawloski is in fact a dual processor system, the reference demonstrates the teachings of well-known techniques where a microcomputer includes provisions for accessing emulation and external memory via an external bus. (Abstract, Summary of Invention, CL1-L49, CL10-L3, CL4-L24, CL4-L43-66 Figs. 1, 2, 5d)*

*Pawloski mentions, but does not explicitly teach the concept of running code (accessing) from different memories based on a selected "**mode**" after system reset.*

*Gephardt teaches the concept of restricting local processor access to certain regions of memory via a "lock-out" register, and then running code in a predetermined portion of memory after system boot (reset). (CL2-L45-64) Gephardt teaches that in one lock-out mode (normal mode), the system will operate (i.e. access and run code) from a predetermined block of memory (as does the claimed invention when 2nd modes is selected) following a system boot. (i.e. reset) When the lock-out register is set to the emulation mode, the system will run code (operate) from a different block (emulation code) of memory following **system reset**. (Abstract, Summary of Invention, CL2-L45-64, CL8-L31-58, Fig. 2) In addition to being taught by Gephardt, the concept of a processor accessed register to control the selection of memory blocks is obvious and well known in the art. This concept is also taught by Pawloski as previously cited.*

*It would have been obvious to one of ordinary skill in the art at the time the claimed invention was made to modify the teachings of Pawloski relating to a microcomputer having an **internal memory** that also accesses an **external bus**, which includes an **mulation memory** and an external (RAM) memory, with the teachings of*

Gephardt relating to restricting local processor access to certain regions of memory and then running (accessing) code in a predetermined portion of memory after system reset to realize the claimed invention. An obvious motivation exists since this area of technology is highly competitive with many emulation systems available in the market place and large amounts of money being spent in product development and improvement. (See Gephardt column 2, line 32, for example) Accordingly, a skilled artisan would have made an effort to become aware of what capabilities had already been developed in the market place and, hence, would have been motivated to modify the teachings of Pawloski with the teachings of Gephardt in order to reduce development time and cost.

Claims 21-23, 25-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 4,939,637 issued to Pawlowski in view of of U.S. Patent 5,623,673 issued to Gephardt et al.

Dependent claims 21-23, 25-28 are drawn to:
Mode** selection **terminal for emulation mode
***Mode selection register** (processor on/off control)*
*Processor **address bus connected to external address bus** and **data bus internal** independent of mode, **connected to external data bus** when emulation **mode on***
Second memory control includes second memory read active before first memory read
Mode selection (third) selecting memory used after reset, and memory transmit (forth)

*Regarding dependent claims 21-23, 25-28: Pawloski teaches the use of a **"mode" selection register** that allows the processor to select emulation mode and further discloses a "pin" (terminal) where the signal is made available. (Fig. 5, 6, CL3-L61-66, CL10-L38-68) This implementation is commonly used in the art.*

It would have been obvious to connect the processor ***address bus conn cted directly to th external address bus*** *(claim 23) since the address lines are not bi-directional and, hence, need not be buffered, and the memory selection is performed independent of the address bus. The practice is also very common in the art since fewer (not needed) components are required.*

It further have been obvious, and necessary, to have the processor ***data bus connected to external data bus*** *when emulation* ***mode on****, since bi-directional data must flow between the processor and the emulation memory via the external data bus.*

It would also have been obvious, and necessary, to have the second memory read active control occur before first memory read since not doing so would result in a "collision" condition between read cycles of the memories.

*Pawloski does not explicitly teach the concept of running code (accessing) from different memories based on a selected "***mode***" after system reset.*

Gephardt teaches the concept of restricting local processor access to certain regions of memory via a "lock-out" register, and then running code in a predetermined portion of memory after system boot (reset). (CL2-L45-64) Gephardt teaches that in one lock-out mode (normal mode), the system will operate (i.e. access and run code) from a predetermined block of memory (as does the claimed invention when 2nd modes is selected) following a system boot. (i.e. reset) When the lock-out register is set to the emulation mode, the system will run code (operate) from a different block (emulation code) of memory following ***system reset****. (Abstract, Summary of Invention, CL2-L45-64, CL8-L31-58, Fig. 2) In addition to being taught by Gephardt, the concept of a*

processor accessed register to control the selection of memory blocks is obvious and well known in the art. (Pawloski Figs. 2, 3 and Gephardt Fig. 2) The use of Internal and external microprocessor busses and a processor controlled means of selecting memory is obvious and well known and common to many modern microprocessor based system as is demonstrated by prior art.

It would have been obvious to one of ordinary skill in the art at the time the claimed invention was made to modify the teachings of Pawloski relating to the use of a ***"mode" selection register*** *that allows the processor to select emulation mode, with the teachings of Gephardt relating to restricting local processor access to certain regions of memory and then running (accessing) code in a predetermined portion of memory* ***after system reset*** *to realize the claimed invention. An obvious motivation exists since this area of technology is highly competitive with many emulation systems available in the market place and large amounts of money being spent in product development and improvement. (See Gephardt column 2, line 32, for example) Accordingly, a skilled artisan would have made an effort to become aware of what capabilities had already been developed in the market place and, hence, would have been motivated to modify the teachings of Pawloski with the teachings of Gephardt in order to reduce development time and cost.*

Allowable Subject Matter

6. Claim 1 uses "mean for" language and are given deference in view of In re Donaldson and interpreted in view of 35 U.S.C. § 112 paragraph 6. The "means for"

language and the limitations (bus control means and memory control means) related thereto of claim 1 is interpreted within the scope of enablement as provided within the relative embodiment provided within applicant's specification. Claims 2-4, and 6-18 are allowable as being dependent from claim 1.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure, careful consideration should be given prior to applicant's response to this Office Action.

U.S. Patent 5,781,750 issued to Blomgren teaches emulation mode and register control.

U.S. Patent 5,062,034 issued to Bakker teaches multiple microcontroller bond-out.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fred Ferris whose telephone number is 703-305-9670 and whose normal working hours are 8:30am to 5:00pm Monday to Friday.

Any inquiry of a general nature relating to the status of this application should be directed to the group receptionist whose telephone number is 703-305-3900.

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